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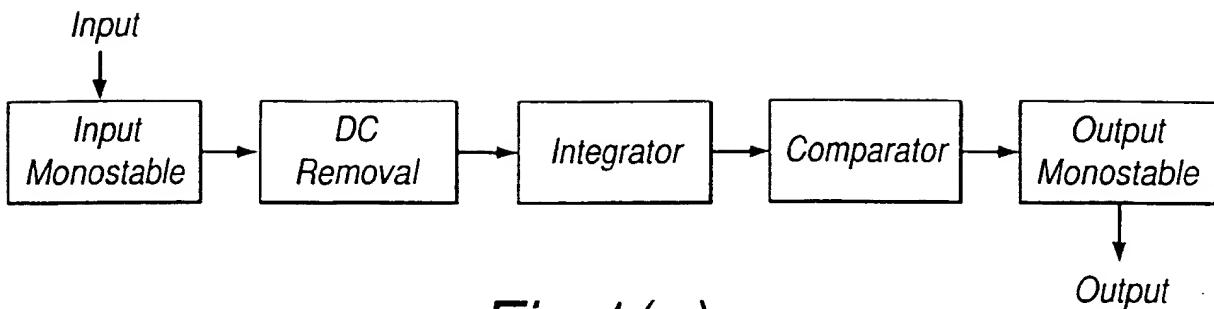


Fig.1(a)

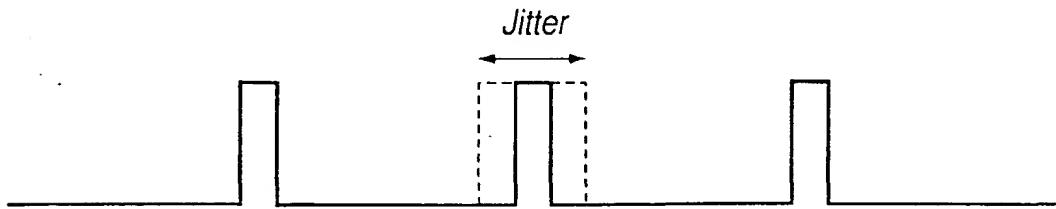


Fig.1(b)

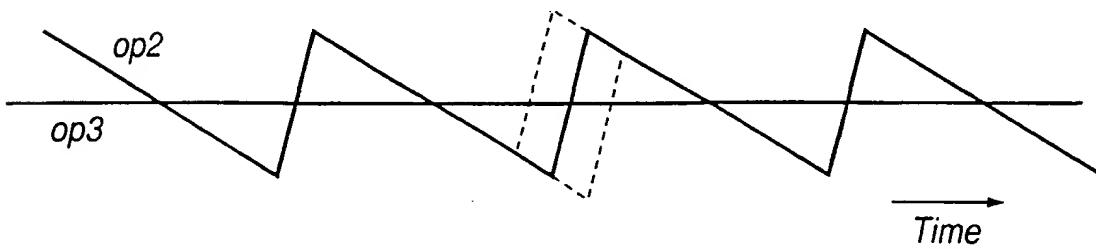


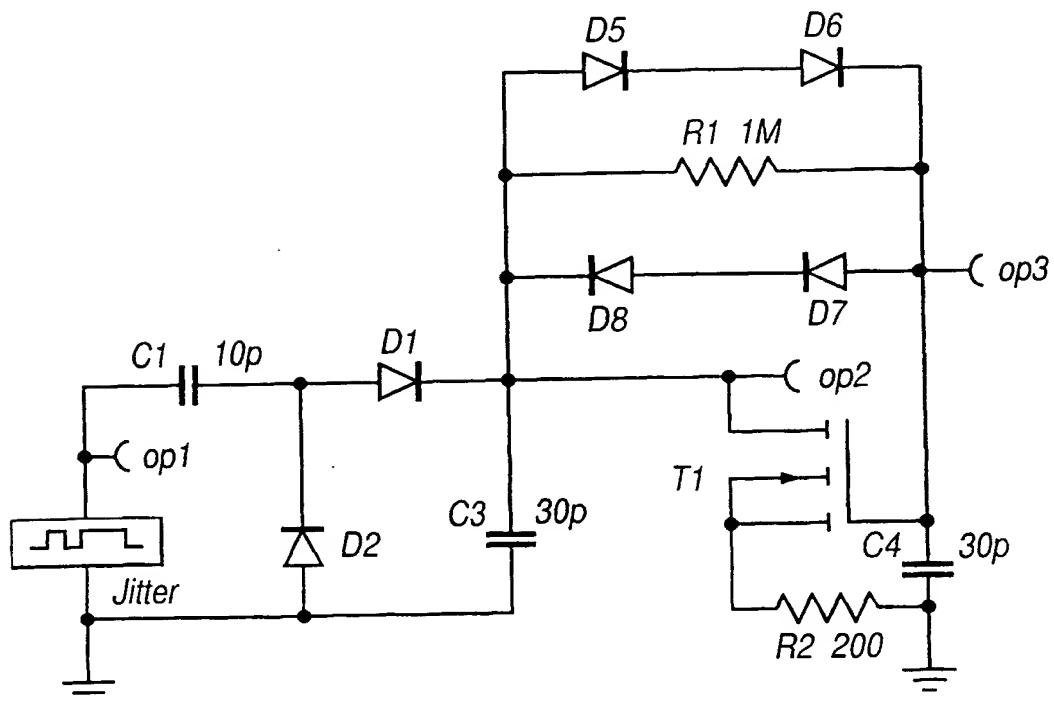
Fig.1(c)

Fig.1 Anti Jitter Circuit Principle:-

- (a) Basic Block Diagram
- (b) Input with jitter on central pulse
- (c) Integrator output (op2) and Comparator switching level (op3)

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T1:- n-MOS enhancement
Threshold 0v Beta 300uA/VV

op2 and op3 to differential comparator

Mean Fin = 417kHz and 1/3 rate phase jumps of 150 degrees
= Time Jitter of 1 usec in 2.4usec at 1/3 rate

Fig.2(a)

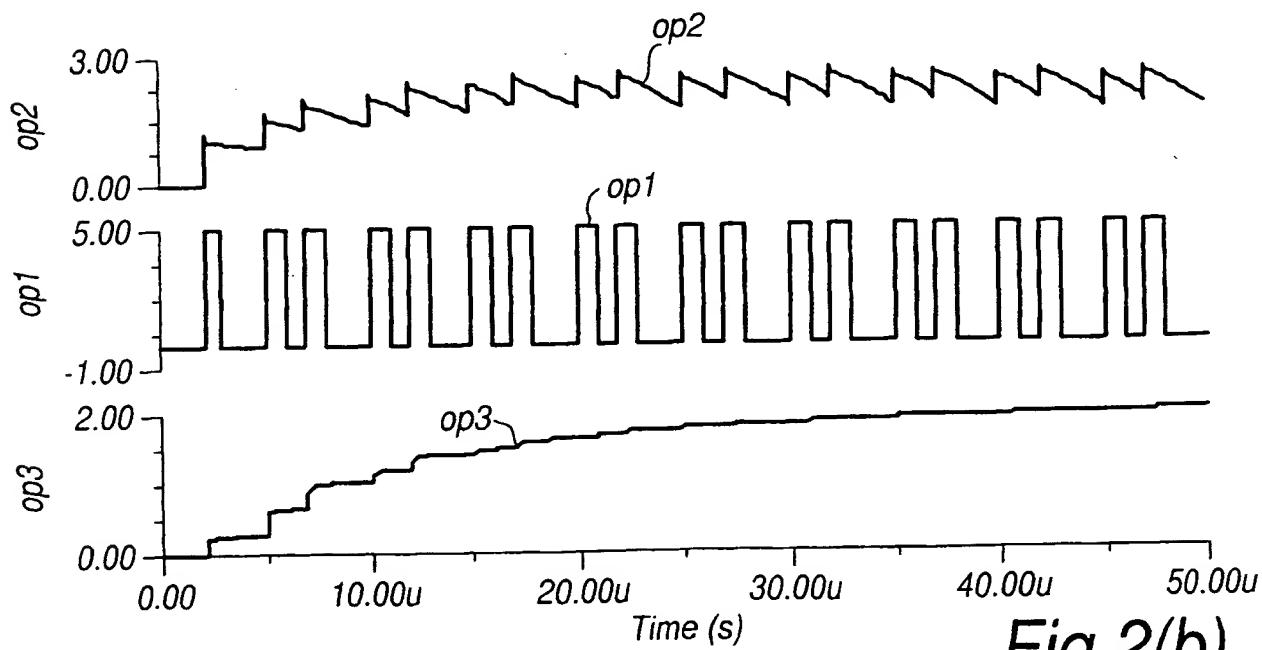


Fig.2(b)

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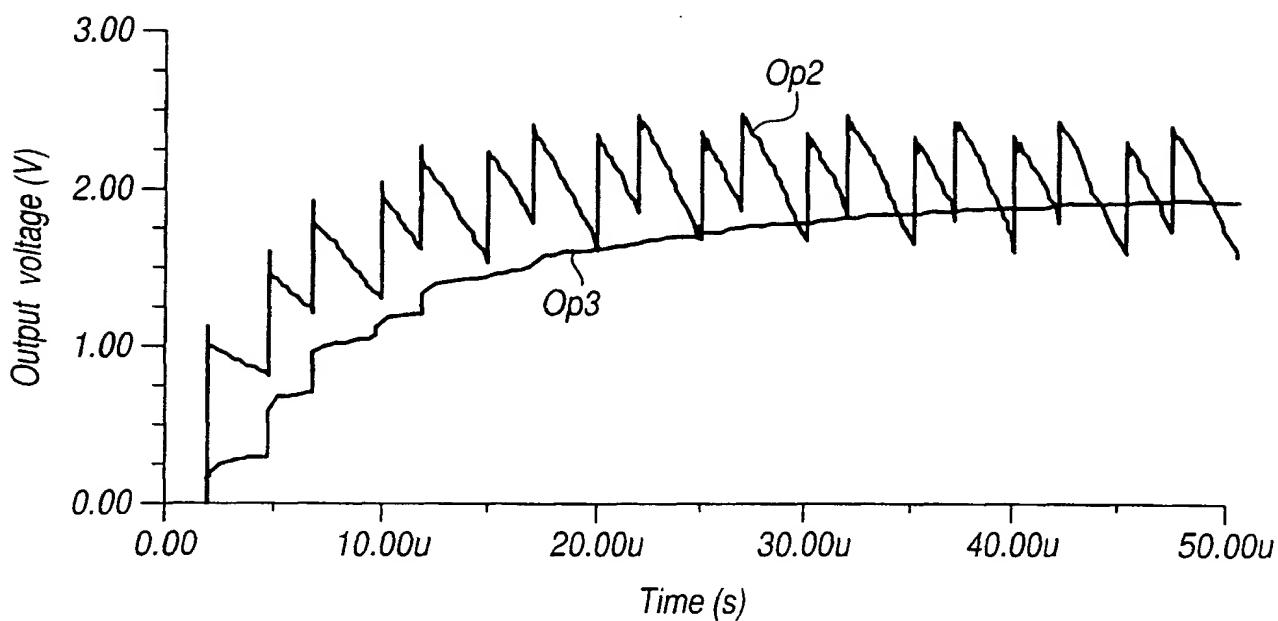


Fig.2(c)

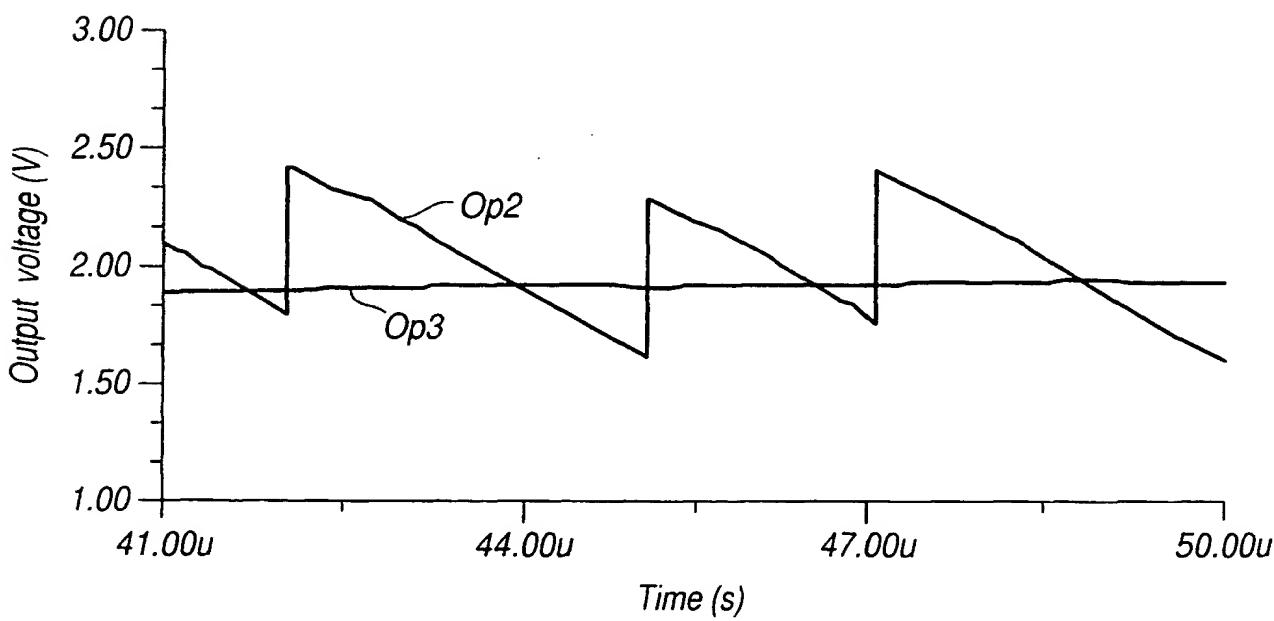


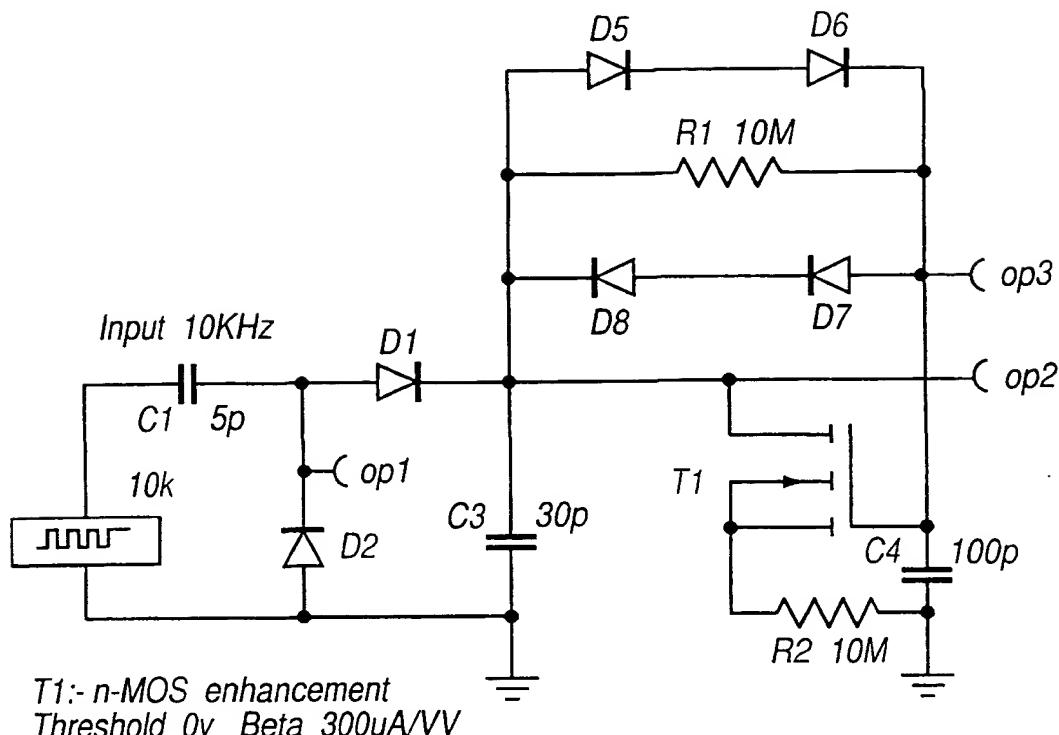
Fig.2(d)

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op2 and op3 to differential comparator

Fig.3(a)

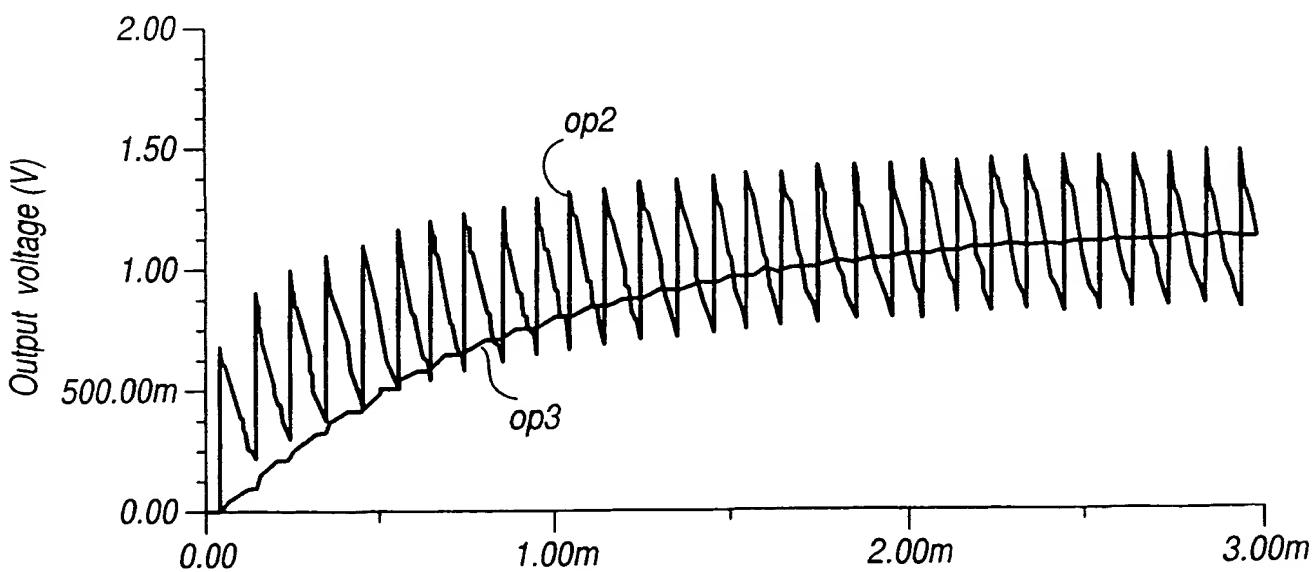
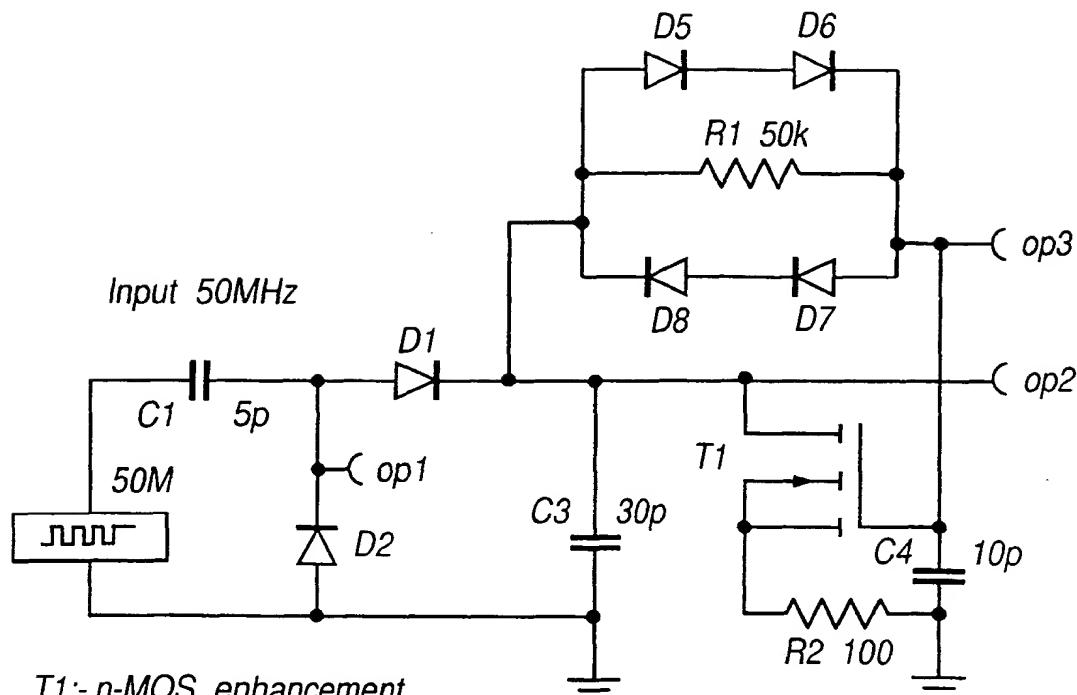


Fig.3(b)

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op2 and op3 to differential comparator

Fig.4(a)

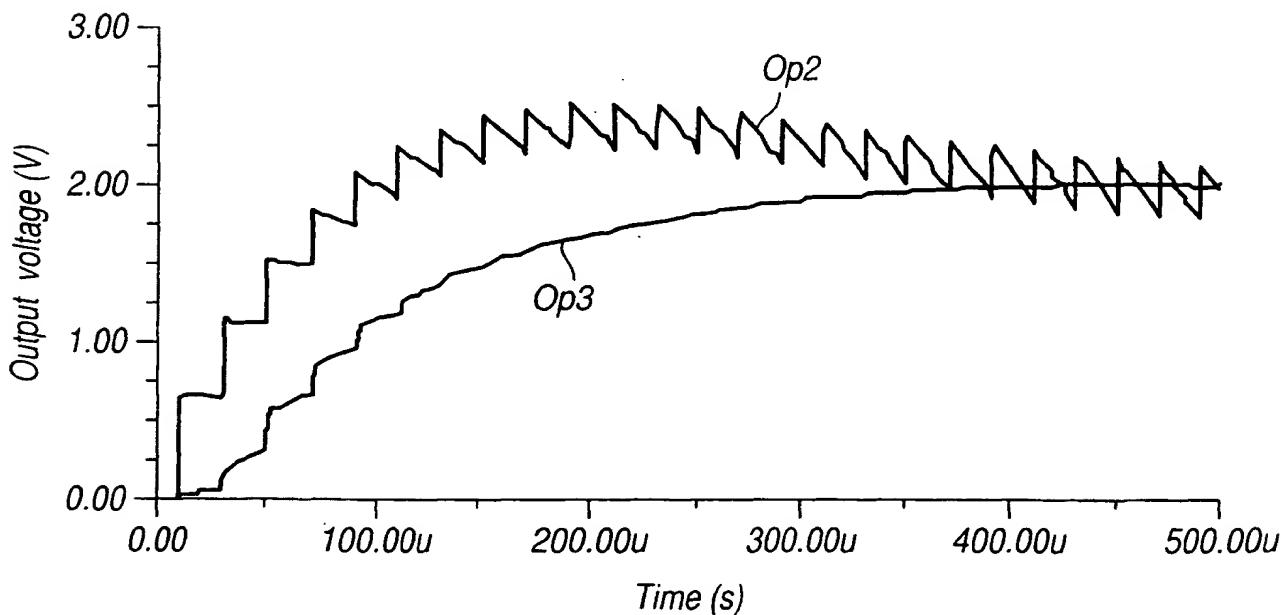
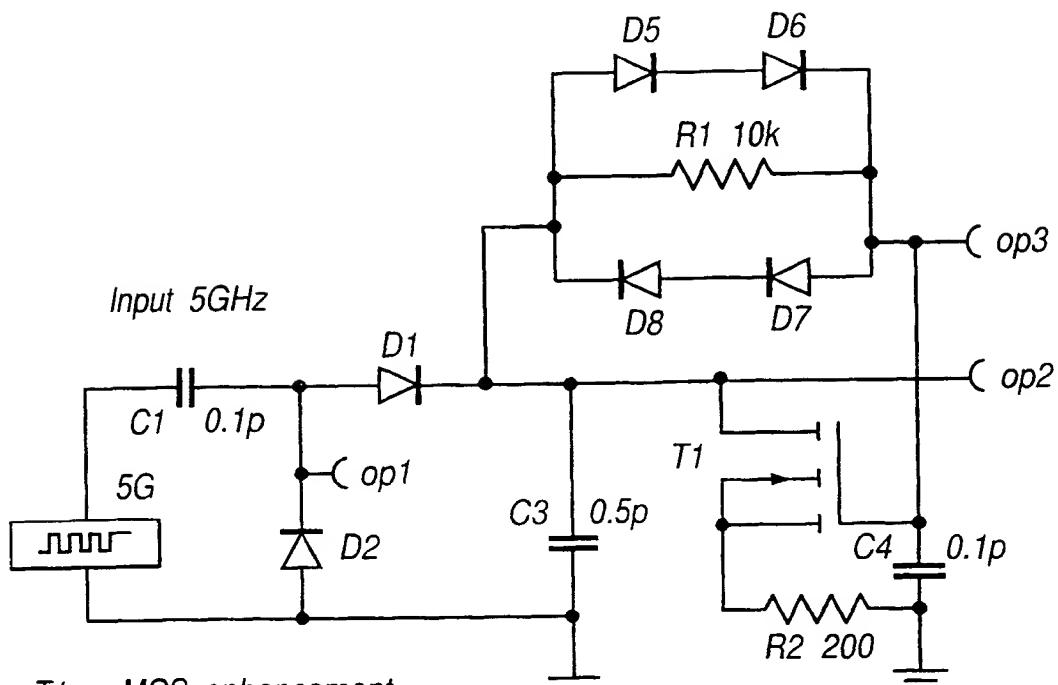


Fig.4(b)

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T_1 : n-MOS enhancement
Threshold 0v Beta 300 μ A/VV

op_2 and op_3 to differential comparator

Fig.5(a)

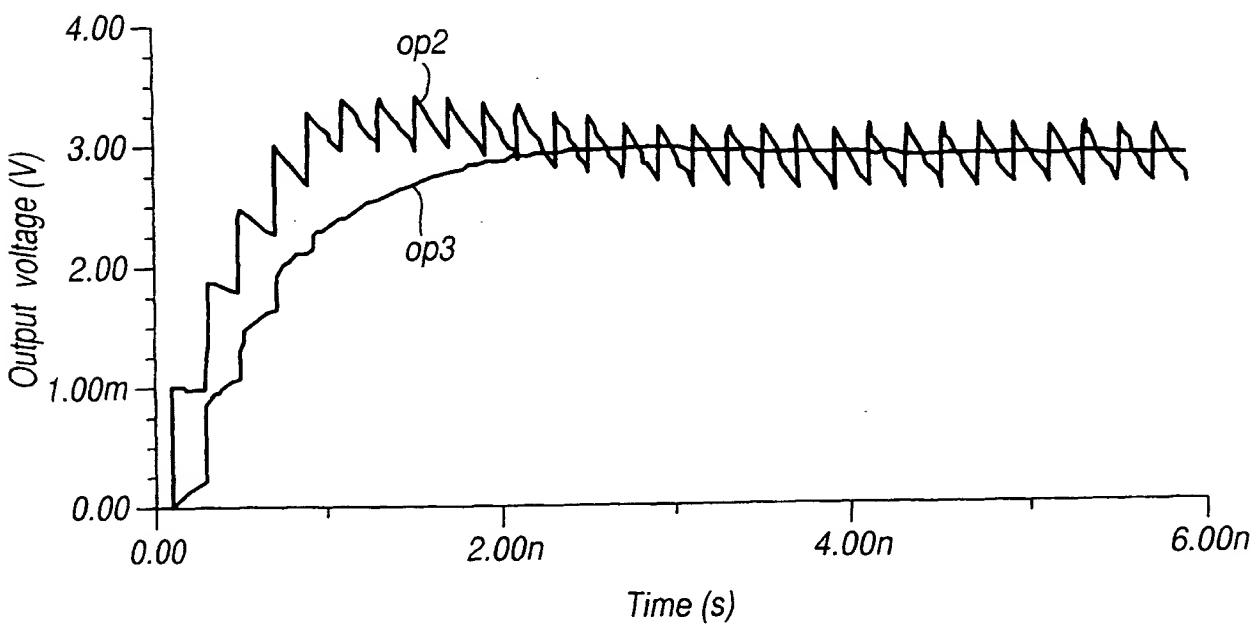


Fig.5(b)

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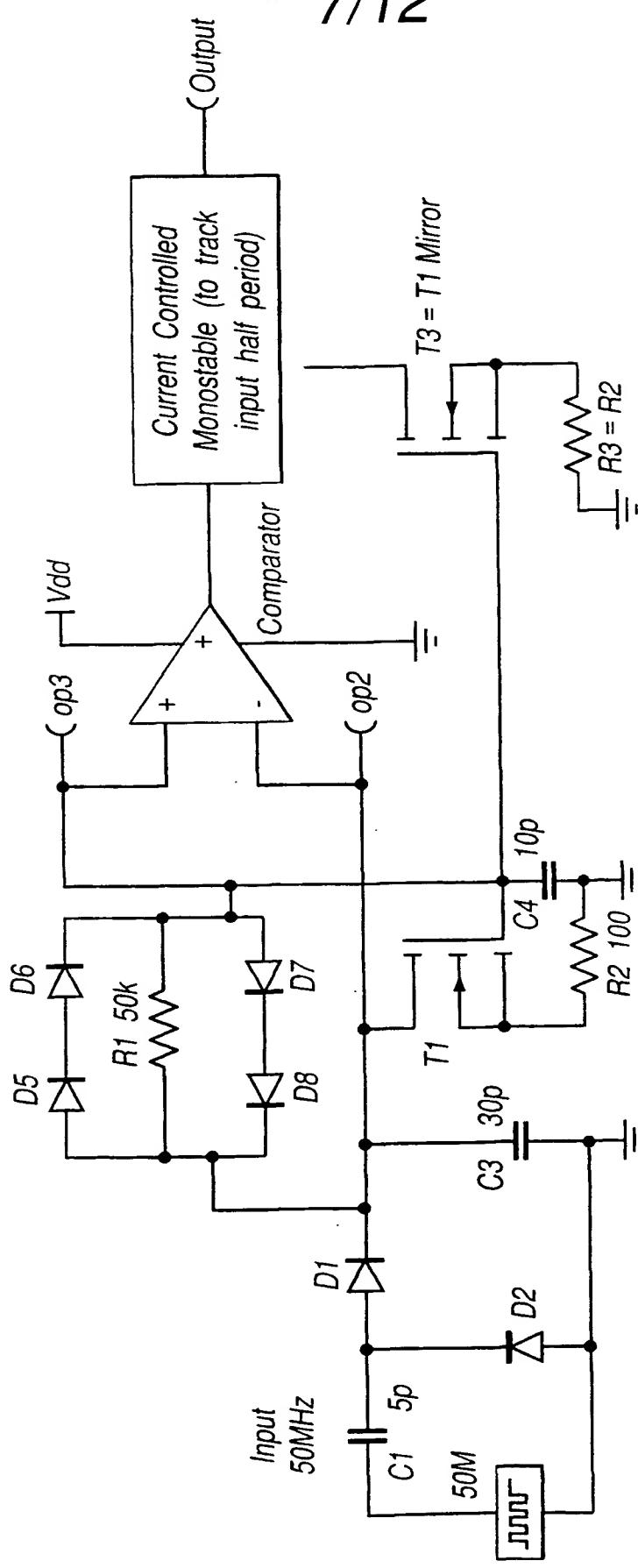
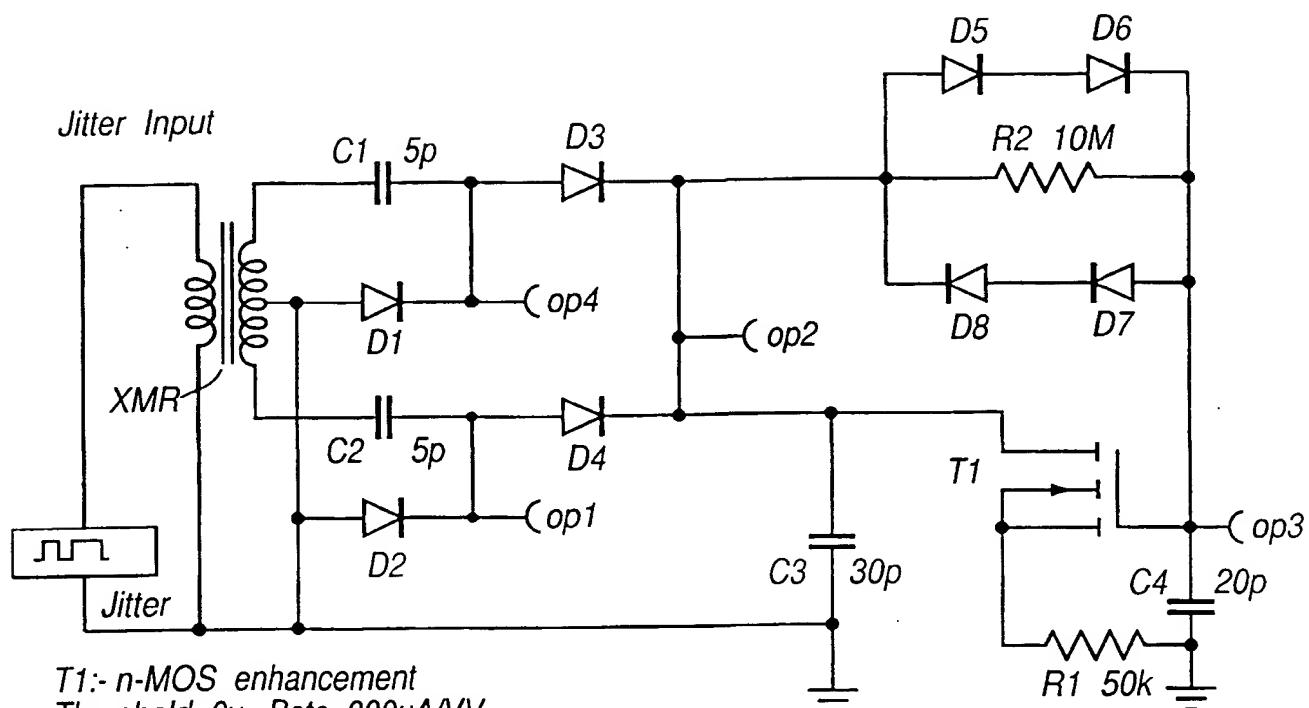


Fig.6

AAJC with Comparator and input-tracking Output Monostable

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Mean Fin = 417kHz and 1/3 rate phase jumps of 150 degrees
= Time Jitter of 1 usec in 2.4 usec at 1/3 rate

Fig.7(a)

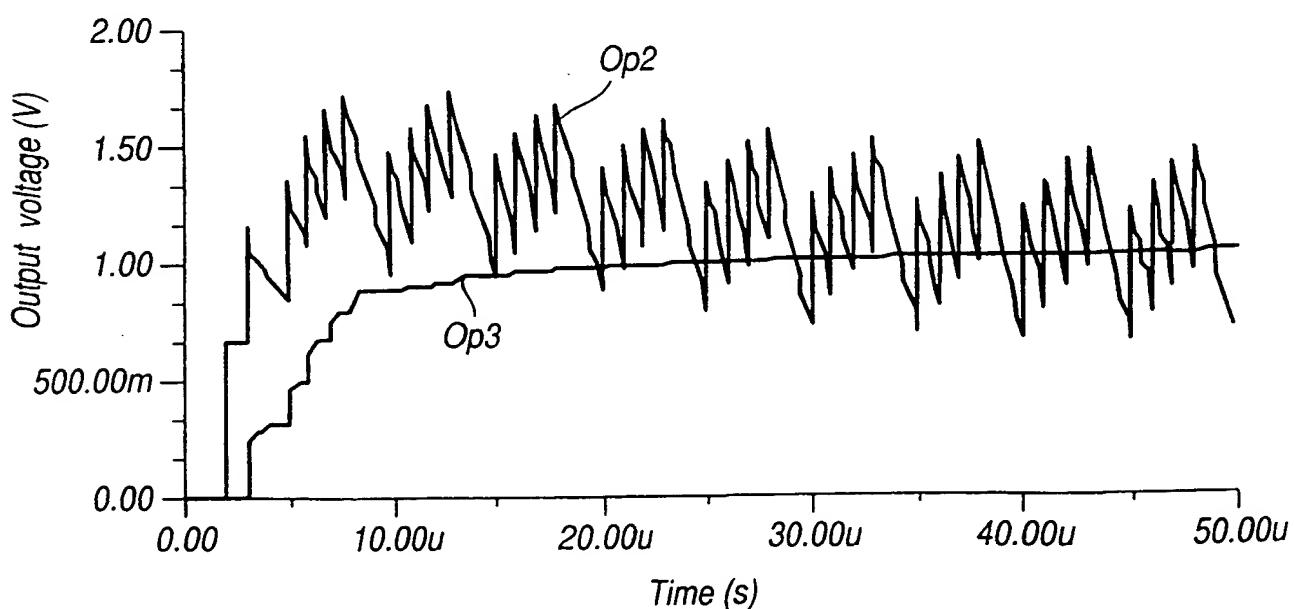


Fig.7(b)

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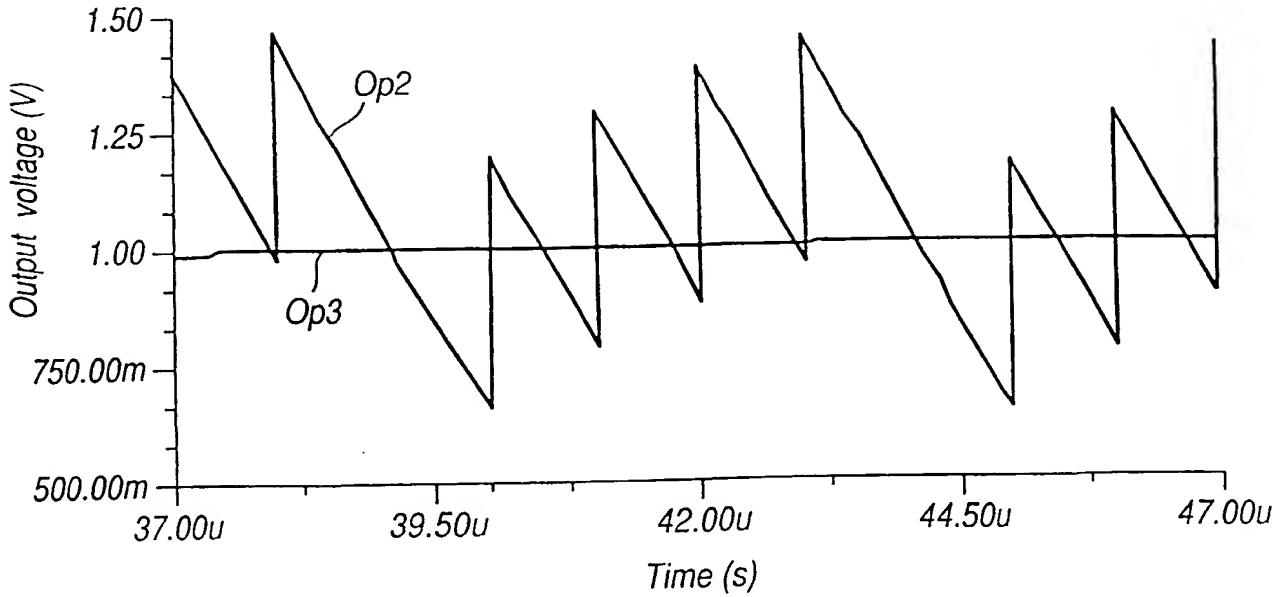
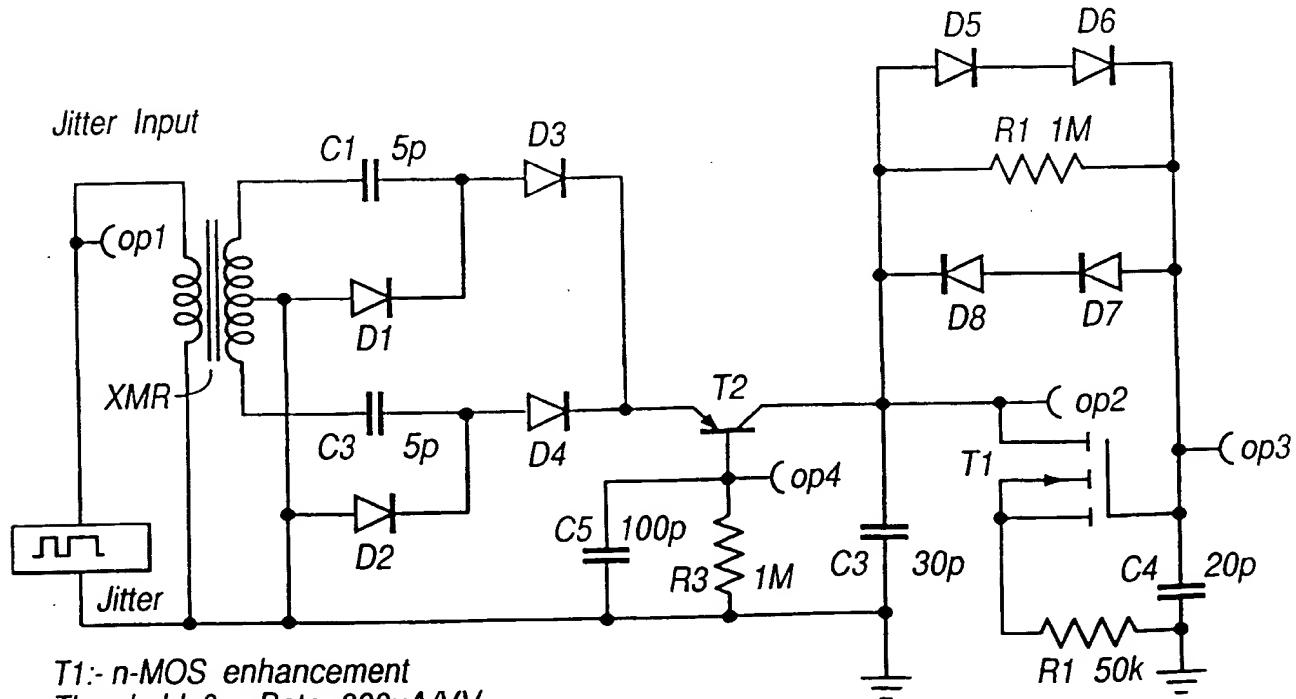


Fig. 7(c)



T1:- n-MOS enhancement
Threshold 0v Beta 300uA/VV

op2 and op3 to differential comparator

Mean Fin = 417kHz and 1/3 rate phase jumps of 150 degrees
= Time Jitter of 1 usec in 2.4 usec at 1/3 rate

Fig.8(a)

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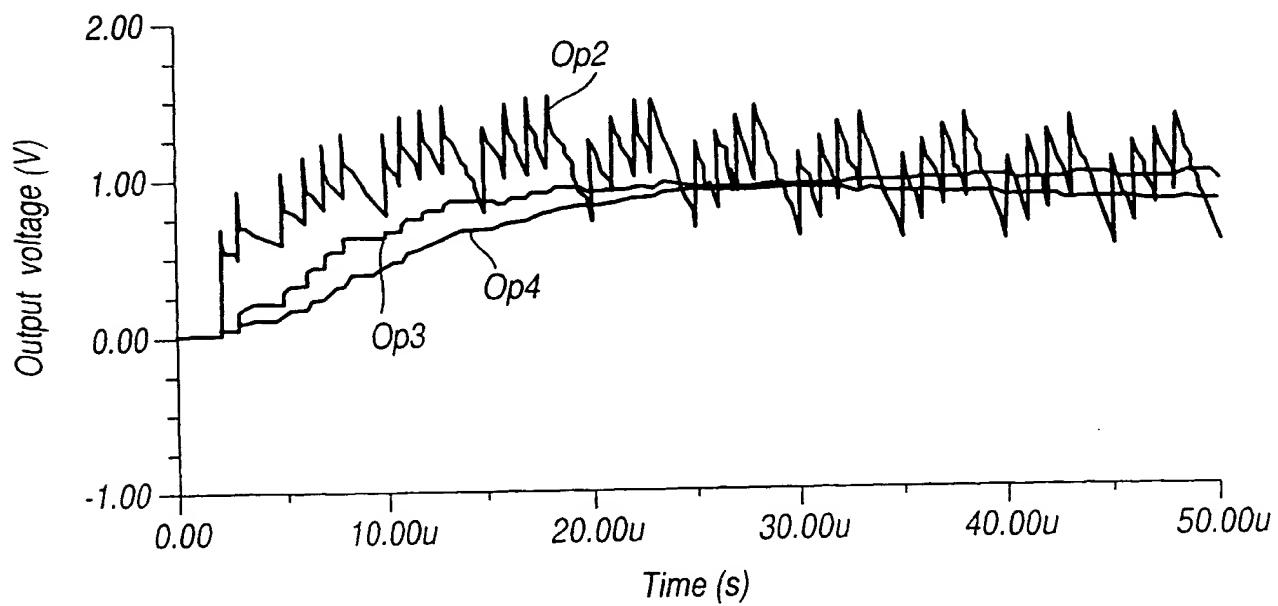


Fig.8(b)

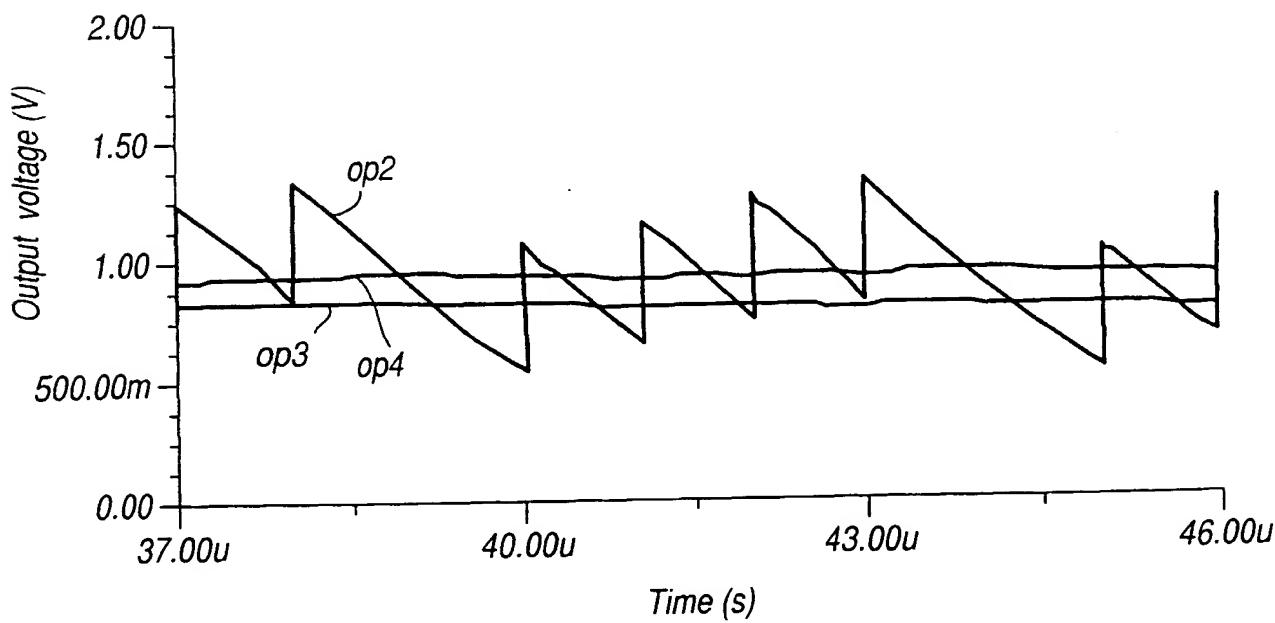


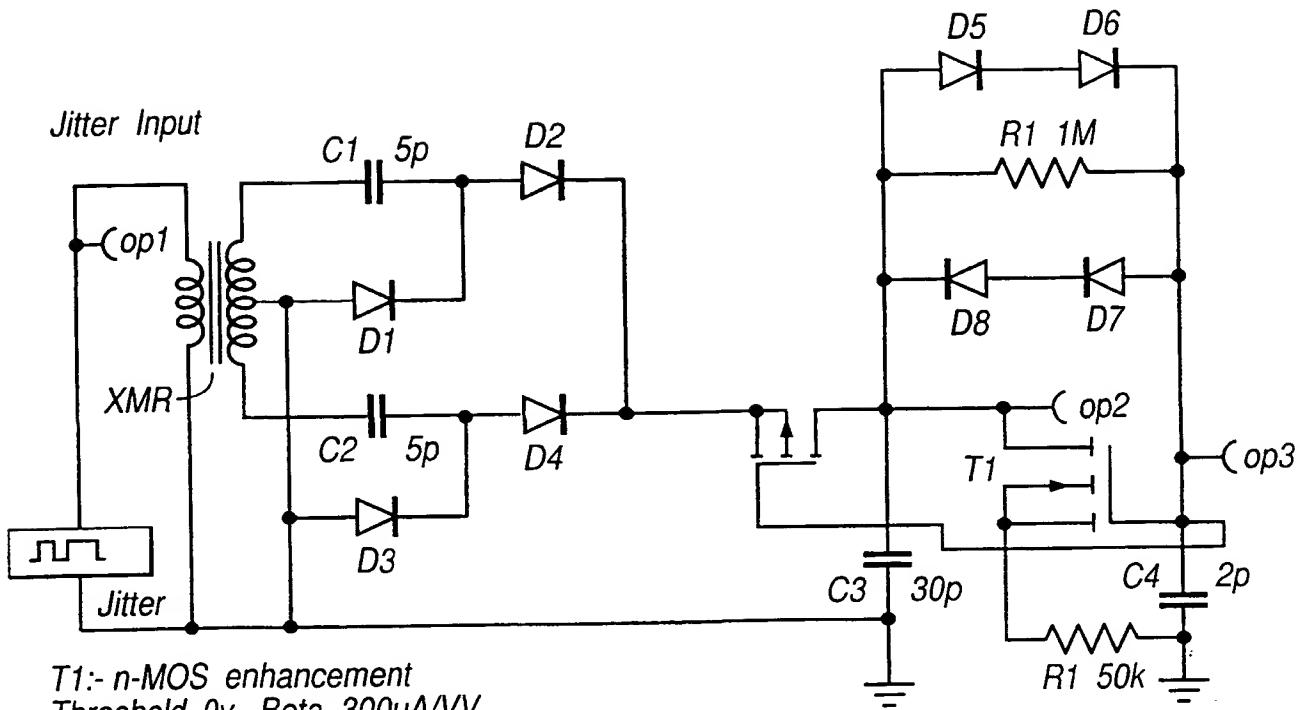
Fig.8(c)

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op2 and op3 to differential comparator

*Mean Fin = 417kHz and 1/3 rate phase jumps of 300 degrees
= Time Jitter of 1 usec in 2.4 usec at 1/3 rate*

Fig.9(a)

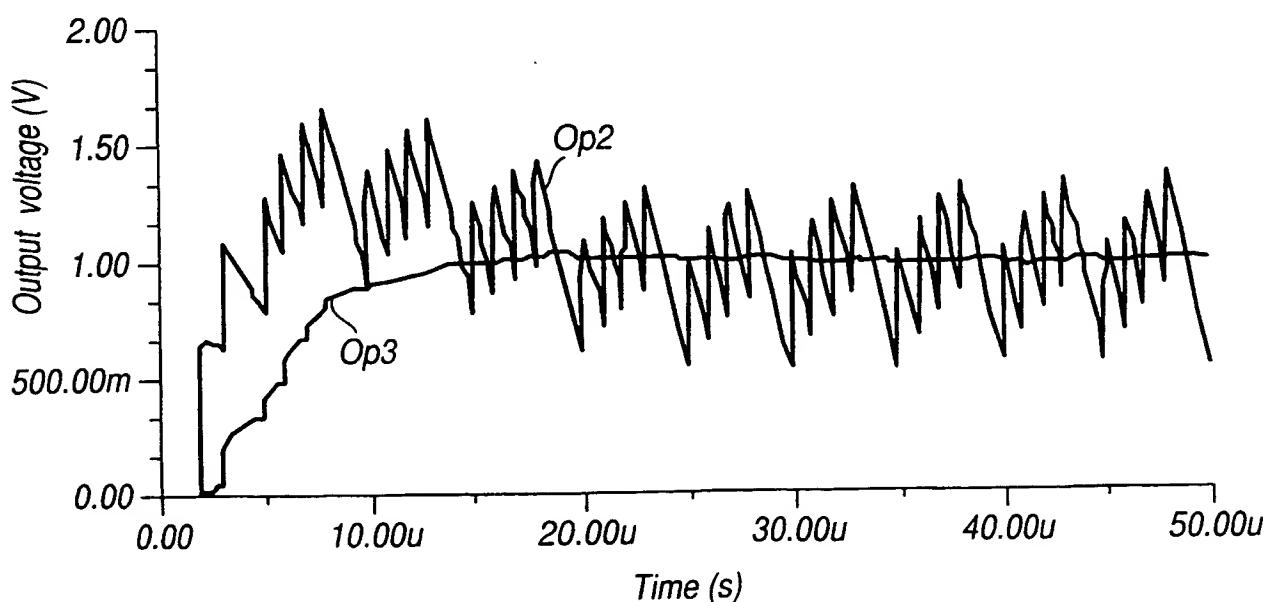


Fig.9(b)

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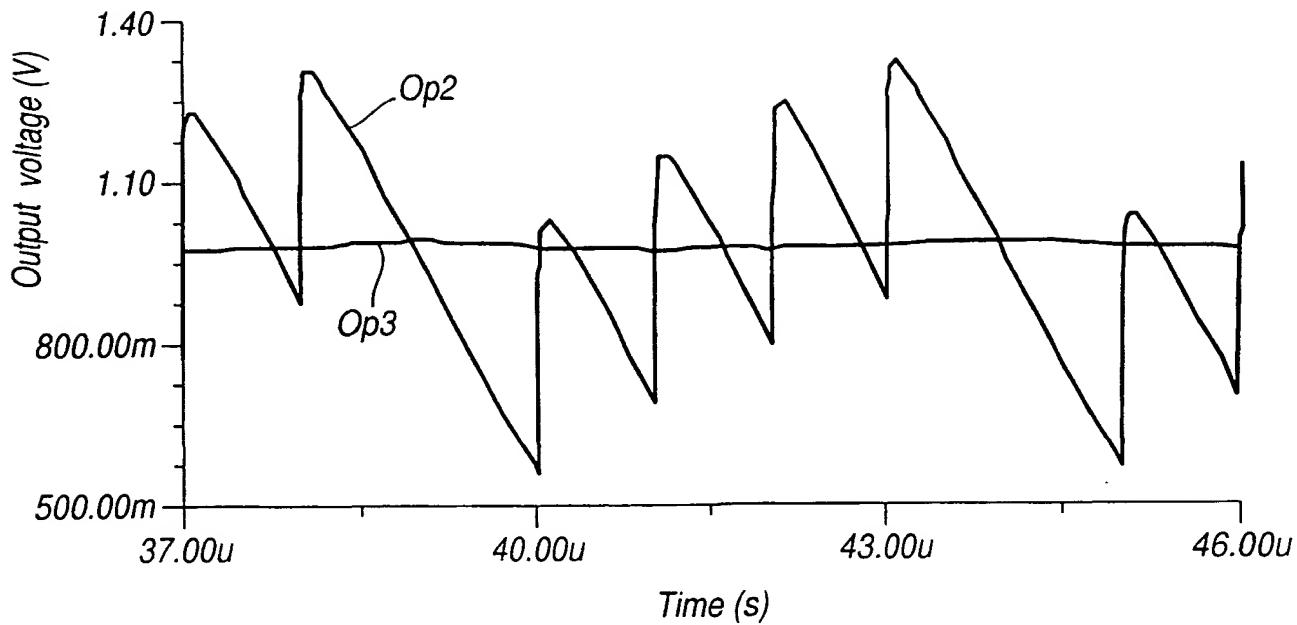


Fig.9(c)

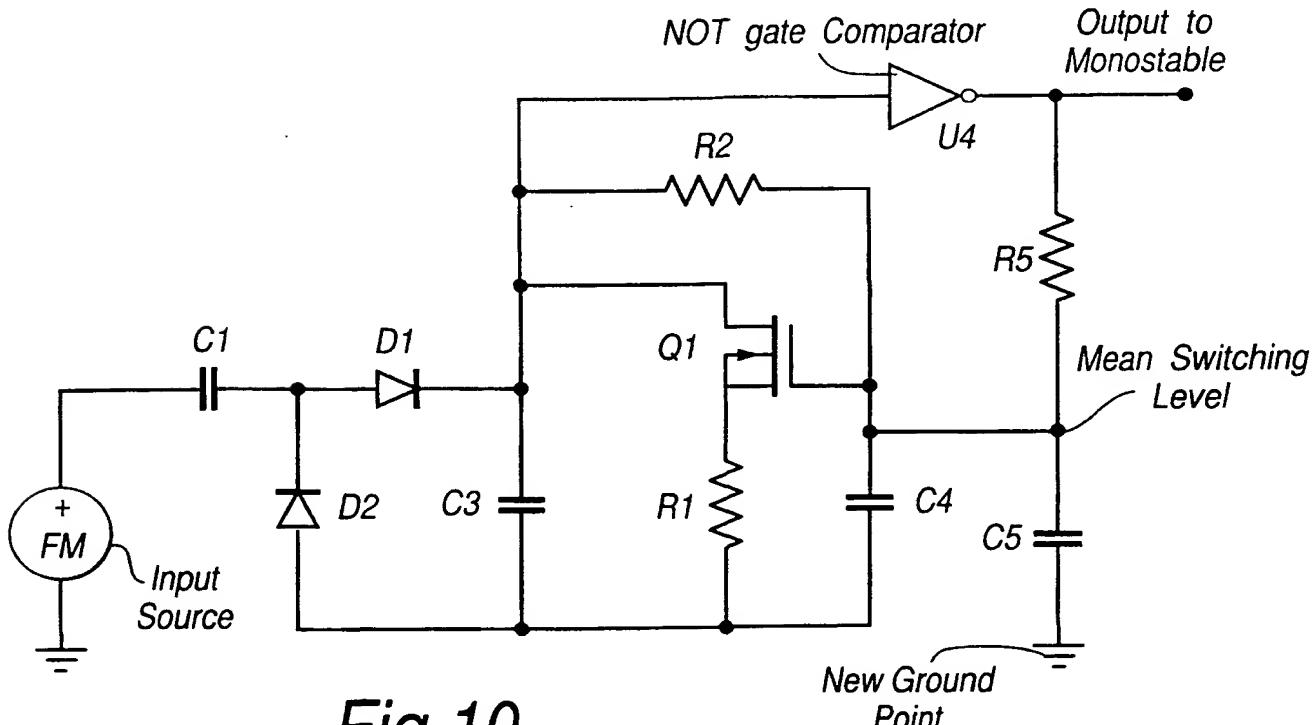


Fig.10